REMARKS

Claims 1-3, 5-6, 11-13, 21-23, and 25-26 were rejected under Section 102(e) over Alston.

Claim 1 calls for receiving a plurality of data units at a source location in a first clock domain. At the first clock domain, an enable signal is detected to control writing of the plurality of data units from the source location to a target location in a second clock domain. The enable signal is then synchronized with respect to the second clock domain. In response to the synchronized enable signal, the plurality of data units are transferred from the first clock domain to a target location in the second clock domain.

Thus, to analyze the claim, with respect to the prior art, it is necessary to know what is the asserted enable signal, and what are the first and second clock domains.

With respect to the rejection of claim 1, contained in paragraph 1, subparagraph a. of the office action, it is not clear exactly what the enable signal is. It is suggested that "detecting an enable signal in the first clock domain to control writing" is found in Figure 1, labeled 152. However, Figure 1, label 152, is an acknowledge signal. Thus, it seems unlikely, if not impossible, that the acknowledge signal could be the claimed enable signal that: 1) controls writing of the plurality of data units from the source location to its target location in the second clock domain, 2) is synchronized with respect to the second clock domain, and 3) results in transferring said plurality of data units from the first clock domain to the target location in the second clock domain. The acknowledgement simply cannot be an enable signal because it is received by the unit that has the data to transfer.

Moreover, with respect to claim 3, the "enabling signal" is asserted to be Figure 1, item 150. See the office action at paragraph 1, subparagraph c. This is the ready signal. Thus, it is unclear what exactly is asserted to be the enable signal set forth in the claim. It is respectfully submitted that it also cannot be the ready signal 150 because the signal 150 is not synchronized. For example, it is suggested that the synchronization is supported by the language at the bottom of column 8, and the top of column 9, but the synchronized signal referred to there is not either the acknowledge signal 150 or the ready signal 152. Thus, neither asserted signal meets the claim limitation of an enable signal synchronized with respect to the second clock domain that controls writing of data units in the first clock domain from a source location to a second location at a second clock domain.

It is also somewhat unclear what are the first and second clocked domains. Therefore, reconsideration is respectfully requested.

Respectfully submitted,

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